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09/823,602	03/30/2001	Joseph Jeddeloh	MIC-4	6053

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CHEN, TSE W	
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2116	3

DATE MAILED: 03/24/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/823,602	JEDDELOH, JOSEPH	
	Examiner	Art Unit	
	Tse Chen	2116	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 March 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-53* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-53* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *23 May 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Drawings

1. The drawings were received on May 23, 2002. These drawings are acceptable.

Specification

2. Claims 33-37 are objected to because of the following informalities: the "said characteristic" in each of the claims 33-37 does not have a corresponding antecedent in the referred claim 31. However, it appears most likely that the applicant may have intended the referring claim to be number 32 instead of 31. Therefore, the Office will perform the examination with claims 33-37 dependent on claim 32 in order to have an appropriate antecedent for "said characteristic". Appropriate correction is still required.

3. Claims 46-50 are objected to because of the following informalities: the "said characteristic" in each of the claims 46-50 does not have a corresponding antecedent in the referred claim 43. However, it appears most likely that the applicant may have intended the referring claim to be number 45 instead of 43. Therefore, the Office will perform the examination with claims 46-50 dependent on claim 45 in order to have an appropriate antecedent for "said characteristic". Appropriate correction is still required.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 9-12, 21-24, 26-32, and 51-53 are rejected under 35 U.S.C. 102(e) as being anticipated by Stevens et al., U.S. Patent 6226729, hereinafter referred to as Stevens.

6. As per claims 9 and 51, Stevens taught an invention to configure memory devices [FIG. 1], the invention comprising of:

- counting the number of memory modules [FIG. 8A, item 850; column 12, lines 62-67; column 13, table 4];
- obtaining information from serial presence detect memory that includes at least one characteristic of the memory module [column 12, lines 2-9]; and
- selecting an operating speed for memory module interface in accordance with at least one of the counting and obtained information [column 13, lines 41-45].

7. As per claim 10, Stevens taught the characteristic comprising of a type of memory module [column 12, lines 8-9].

8. As per claims 11 and 52, Stevens taught an invention to configure memory devices [FIG. 1], the invention comprising of:

- counting the number of memory modules [FIG. 8A, item 850; column 12, lines 62-67; column 13, table 4];
- obtaining information from serial presence detect memory that includes at least the number of components in each memory module [column 12, lines 2-14][1]; and
- selecting an operating speed for memory module interface in accordance with at least one of the counting and obtained information [column 13, lines 41-45].

[1] RIMM SPD Specification Version 1.1 from October 2000 disclosed number of components on a module as located in byte number 99 on a Rambus Serial Presence Detect.

9. As per claims 12 and 53, Stevens taught an invention to configure memory devices [FIG. 1], the invention comprising of:

- counting the number of memory modules [FIG. 8A, item 850; column 12, lines 62-67; column 13, table 4];
- obtaining information from serial presence detect memory that includes at least the speed grade of the memory module [column 12, lines 2-14][2]; and
- selecting an operating speed for memory module interface in accordance with at least one of the counting and obtained information [column 13, lines 41-45].

10. As per claims 21 and 26, Stevens taught an invention to configure memory devices [FIG. 1], the invention comprising of:

- a central processing unit [FIG. 5, item 595];
- a memory controller including a memory module interface [FIG. 5, item 500]; and
- at least one memory module including a serial presence detect memory [FIG. 5, items 570 and 572];
- wherein the memory controller:
    - accesses the serial presence detect memory [column 2, lines 2-9];
    - keeps a running tally of the number of memory modules based on accesses to serial presence detect memory [FIG. 8A, item 850; column 12, lines 62-67; column 13, table 4];
    - obtains information from serial presence detect memory that includes at least one characteristic of the memory module [column 12, lines 2-9]; and

- selects an operating speed for memory module interface in accordance with at least one of a final tally of the number of memory modules and obtained information [column 13, lines 41-45].

11. As per claim 22, Stevens taught the characteristic comprising of the number of components in each memory module [column 12, lines 2-14][3].

12. As per claims 23 and 29, Stevens taught an invention to configure memory devices [FIG. 1], the invention comprising of:

- a central processing unit [FIG. 5, item 595];
- a memory controller including a memory module interface [FIG. 5, item 500]; and
- at least one memory module including a serial presence detect memory [FIG. 5, items 570 and 572];
- wherein the memory controller:
  - accesses the serial presence detect memory [column 2, lines 2-9];
  - keeps a running tally of the number of memory modules based on accesses to serial presence detect memory [FIG. 8A, item 850; column 12, lines 62-67; column 13, table 4];
  - obtains information from serial presence detect memory that includes at least the number of components in each memory module [column 12, lines 2-14][4]; and

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[2] RIMM SPD Specification Version 1.1 from October 2000 disclosed various speed information for a module (e.g., byte numbers 10 –37) on a Rambus Serial Presence Detect.
[3] RIMM SPD Specification Version 1.1 from October 2000 disclosed number of components on a module as located in byte number 99 on a Rambus Serial Presence Detect.
[4] RIMM SPD Specification Version 1.1 from October 2000 disclosed number of components on a module as located in byte number 99 on a Rambus Serial Presence Detect.

- selects an operating speed for memory module interface in accordance with at least one of a final tally of the number of memory modules and obtained information [column 13, lines 41-45].

13. As per claim 24 and 30, Stevens taught an invention to configure memory devices [FIG. 1], the invention comprising of:

- a central processing unit [FIG. 5, item 595];
- a memory controller including a memory module interface [FIG. 5, item 500]; and
- at least one memory module including a serial presence detect memory [FIG. 5, items 570 and 572];
- wherein the memory controller:
  - accesses the serial presence detect memory [column 2, lines 2-9];
  - keeps a running tally of the number of memory modules based on accesses to serial presence detect memory [FIG. 8A, item 850; column 12, lines 62-67; column 13, table 4];
  - obtains information from serial presence detect memory that includes at least the speed grade of the memory module [column 12, lines 2-14][5]; and
  - selects an operating speed for memory module interface in accordance with at least one of a final tally of the number of memory modules and obtained information [column 13, lines 41-45].

14. As per claim 27, Stevens taught the characteristic comprising of a type of memory module [column 12, lines 8-9].

15. As per claim 28, Stevens taught the characteristic comprising of a physical layout of signal connections between memory controller means and memory module means [column 12, lines 8].

16. As per claim 31, Stevens taught an invention to configure memory devices [FIG. 1], the invention comprising of a memory controller including a memory module interface [FIG. 5, item 500] with a serial presence detect memory [FIG. 5, items 570 and 572], wherein the memory controller:

- accesses the serial presence detect memory [column 2, lines 2-9];
- keeps a running tally of the number of memory modules based on accesses to serial presence detect memory [FIG. 8A, item 850; column 12, lines 62-67; column 13, table 4]; and
- selects an operating speed for memory module interface in accordance with at least a final tally of the number of memory modules [column 13, lines 41-45].

17. As per claim 32, Stevens taught obtaining information from serial presence detect memory that includes at least one characteristic of the memory module [column 12, lines 2-9] and basing the operating speed for memory module interface also on obtained information [column 13, lines 41-45].

18.

Claim Rejections - 35 USC § 103

19. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

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[5] RIMM SPD Specification Version 1.1 from October 2000 disclosed various speed information for a module (e.g.,

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

20. Claims 1-5, 7-8, 43-47, and 49-50 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens et al., U.S. Patent 6226729, hereinafter referred to as Stevens, in view of Johnson et al., U.S. Patent 5577236, hereinafter referred to as Johnson.

21. As per claims 1 and 43, Stevens taught an invention to configure memory devices [FIG. 1], the invention comprising of:

- counting the number of memory modules [FIG. 8A, item 850; column 12, lines 62-67; column 13, table 4]; and
- selecting an operating speed for memory module interface in accordance with the counting [column 13, lines 41-45].

22. However, Stevens did not expressly disclose generating multiple clock frequencies to be selected or the reading of data from the memory modules.

23. Johnson taught an invention to read from a variable number of memory devices [FIG. 3], the invention comprising of generating multiple clock frequencies to provide selectable operating speeds for the memory module interface [FIG. 4; column 7, lines 34-39; lines 53-59].

24. An ordinary artisan at the same time the invention was made would have been motivated to look for a way to accurately read data from a memory that may vary in numbers and other attributes [see Johnson: column 2, line 46 to column 3, line 50]. Generating multiple clock frequencies to be ready for selection would also alleviate any transitional delays associated with decreasing or increasing a current frequency to the desired frequency.

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byte numbers 10 –37) on a Rambus Serial Presence Detect.

25. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Stevens and Johnson because of the aforementioned motivations and also their involvement in similar problems regarding the configuration and operation of a system comprising of a variable number of memory devices.

26. As per claims 2 and 44, Stevens taught the selecting comprising of generating memory module interface signals comprising of clock, address, and data signals at a frequency based on memory module count [column 5, lines 11-16; column 13, lines 41-56].

27. As per claims 3 and 45, Johnson taught obtaining characteristic of memory module from serial presence detect memory and selecting one of operating speeds in accordance with characteristic and module count [column 8, lines 33-45; column 9, lines 4-18].

28. As per claims 4 and 46, Johnson taught the characteristic comprising of the number of components in a memory module [column 9, lines 9-10].

29. As per claims 5 and 47, Johnson taught the characteristic comprising of a speed grade of memory module [column 9, lines 17-18].

30. As per claims 7 and 49, Johnson taught the characteristic comprising of a type of memory module [column 8, line 39].

31. As per claims 8 and 50, Johnson, taught the characteristic comprising of a physical layout of signal connections between memory controller and memory module [column 9, lines 11-16].

32. Claims 6 and 48 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens and Johnson as applied to claim 3 above, and further in view of Olarig et al., U.S. Patent 6134638, hereinafter referred to as Olarig.

33. Stevens and Johnson taught an invention to configure a number of memory devices by selecting an operating frequency based on a counting number of the memory devices and a characteristic obtained from the serial presence detect memory.

34. However, Stevens and Johnson did not expressly disclose the characteristic comprising of a manufacturer identification.

35. Olarig taught an invention to support a number of memory devices with different operating speeds. The invention comprising of serial presence detect memory with characteristic comprising of the manufacturer of the memory module [column 10, table 1].

36. An ordinary artisan at the same time the invention was made would have been motivated to look for a way to utilize the manufacturing information of a memory device to determine the preferable operating conditions [see Olarig: column 10, lines 31-37].

37. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Olarig, Stevens, and Johnson because of the aforementioned motivations and also their involvement in similar problems regarding the configuration and operation of a system comprising of a variable number of memory devices.

38. Claims 13-17, 19-20, 25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens et al., U.S. Patent 6226729, hereinafter referred to as Stevens, in view of Johnson et al., U.S. Patent 5577236, hereinafter referred to as Johnson.

39. As per claims 13-14 and 25, Stevens taught an invention to configure memory devices [FIG. 1], the invention comprising of:

- a central processing unit [FIG. 5, item 595];

- a memory controller including a memory module interface [FIG. 5, item 500]; and
- at least one memory module including a serial presence detect memory [FIG. 5, items 570 and 572];
- wherein the memory controller:
    - accesses the serial presence detect memory [column 2, lines 2-9];
    - keeps a running tally of the number of memory modules based on accesses to serial presence detect memory [FIG. 8A, item 850; column 12, lines 62-67; column 13, table 4]; and
    - selects an operating speed for the memory module interface in accordance with at least a final tally of the number of memory modules [column 13, lines 41-45].

40. However, Stevens did not expressly disclose generating multiple clock frequencies to be selected or the reading of data from the memory modules.

41. Johnson taught an invention to read from a variable number of memory devices [FIG. 3], the invention comprising of generating multiple clock frequencies to provide selectable operating speeds for the memory module interface [FIG. 4; column 7, lines 34-39; lines 53-59].

42. An ordinary artisan at the same time the invention was made would have been motivated to look for a way to accurately read data from a memory that may vary in numbers and other attributes [see Johnson: column 2, line 46 to column 3, line 50]. Generating multiple clock frequencies to be ready for selection would also alleviate any transitional delays associated with decreasing or increasing a current frequency to the desired frequency.

43. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Stevens and Johnson because of the aforementioned motivations and also their involvement in similar problems regarding the configuration and operation of a system comprising of a variable number of memory devices.

44. As per claim 15, Stevens taught obtaining information from serial presence detect memory that includes at least one characteristic of each memory module [column 12, lines 2-9, 36-42].

45. As per claim 16, Johnson taught the characteristic comprising of the number of components in a memory module [column 9, lines 9-10].

46. As per claim 17, Johnson taught the characteristic comprising of a speed grade of memory module [column 9, lines 17-18].

47. As per claim 19, Johnson taught the characteristic comprising of a type of memory module [column 8, line 39].

48. As per claim 20, Johnson, taught the characteristic comprising of a physical layout of signal connections between memory controller and memory module [column 9, lines 11-16].

49. Claim 18 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens and Johnson as applied to claim 3 above, and further in view of Olarig et al., U.S. Patent 6134638, hereinafter referred to as Olarig.

50. Stevens and Johnson taught an invention to configure a number of memory devices by selecting an operating frequency based on a counting number of the memory devices and a characteristic obtained from the serial presence detect memory.

51. However, Stevens and Johnson did not expressly disclose the characteristic comprising of a manufacturer identification.

52. Olarig taught an invention to support a number of memory devices with different operating speeds. The invention comprising of serial presence detect memory with characteristic comprising of the manufacturer of the memory module [column 10, table 1].

53. An ordinary artisan at the same time the invention was made would have been motivated to look for a way to utilize the manufacturing information of a memory device to determine the preferable operating conditions [see Olarig: column 10, lines 31-37].

54. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Olarig, Stevens, and Johnson because of the aforementioned motivations and also their involvement in similar problems regarding the configuration and operation of a system comprising of a variable number of memory devices.

55. Claims 33-34 and 36-37 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens et al., U.S. Patent 6226729, hereinafter referred to as Stevens, as applied to claim 32 above, and further in view of Johnson et al., U.S. Patent 5577236, hereinafter referred to as Johnson.

56. Stevens taught an invention to configure a number of memory devices by selecting an operating frequency based on a counting number of the memory devices and a characteristic obtained from the serial presence detect memory.

57. However, Stevens did not expressly disclose the specific characteristic to be considered in conjunction with the counting number of memory devices or the reading of data from the memory modules.

58. As per claim 33, Johnson taught the characteristic comprising of the number of components in a memory module [column 9, lines 9-10].

59. As per claim 34, Johnson taught the characteristic comprising of a speed grade of memory module [column 9, lines 17-18].

60. As per claim 36, Johnson taught the characteristic comprising of a type of memory module [column 8, line 39].

61. As per claim 37, Johnson, taught the characteristic comprising of a physical layout of signal connections between memory controller and memory module [column 9, lines 11-16].

62. An ordinary artisan at the same time the invention was made would have been motivated to look for a way to accurately read data from a memory that may vary in numbers and other attributes [see Johnson: column 2, line 46 to column 3, line 50].

63. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Stevens and Johnson because of the aforementioned motivation and also their involvement in similar problems regarding the configuration and operation of a system comprising of a variable number of memory devices.

64. Claim 35 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens as applied to claim 32 above, and further in view of Olarig et al., U.S. Patent 6134638, hereinafter referred to as Olarig.

65. Stevens taught an invention to configure a number of memory devices by selecting an operating frequency based on a counting number of the memory devices and a characteristic obtained from the serial presence detect memory.

66. However, Stevens did not expressly disclose the specific characteristic to be considered in conjunction with the counting number of memory devices or the reading of data from the memory modules.

67. Olarig taught an invention to support a number of memory devices with different operating speeds. The invention comprising of serial presence detect memory with characteristic comprising of the manufacturer of the memory module [column 10, table 1].

68. An ordinary artisan at the same time the invention was made would have been motivated to look for a way to utilize the manufacturing information of a memory device to determine the preferable operating conditions [see Olarig: column 10, lines 31-37].

69. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Olarig and Stevens because of the aforementioned motivations and also their involvement in similar problems regarding the configuration and operation of a system comprising of a variable number of memory devices.

70. Claims 38-39 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens et al., U.S. Patent 6226729, hereinafter referred to as Stevens, in view of Johnson et al., U.S. Patent 5577236, hereinafter referred to as Johnson.

71. As per claim 38, Stevens taught an invention to configure memory devices [FIG. 1], the invention comprising of a memory controller including a memory module interface [FIG. 5, item

500] with a serial presence detect memory [FIG. 5, items 570 and 572], wherein the memory controller:

- accesses the serial presence detect memory [column 2, lines 2-9];
- keeps a running tally of the number of memory modules based on accesses to serial presence detect memory [FIG. 8A, item 850; column 12, lines 62-67; column 13, table 4];
- obtains information from serial presence detect memory that includes at least one characteristic of the memory module [column 12, lines 2-9]; and
- selects an operating speed for memory module interface in accordance with at least one of a final tally of the number of memory modules and obtained information [column 13, lines 41-45].

72. However, Stevens did not expressly disclose generating multiple clock frequencies to be selected or the reading of data from the memory modules.

73. Johnson taught an invention to read from a variable number of memory devices [FIG. 3], the invention comprising of generating multiple clock frequencies to provide selectable operating speeds for the memory module interface [FIG. 4; column 7, lines 34-39; lines 53-59].

74. An ordinary artisan at the same time the invention was made would have been motivated to look for a way to accurately read data from a memory that may vary in numbers and other attributes [see Johnson: column 2, line 46 to column 3, line 50]. Generating multiple clock frequencies to be ready for selection would also alleviate any transitional delays associated with decreasing or increasing a current frequency to the desired frequency.

75. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Stevens and Johnson because of the aforementioned motivations and also their involvement in similar problems regarding the configuration and operation of a system comprising of a variable number of memory devices.

76. As per claim 39, Johnson taught the characteristic comprising of a speed grade of memory module [column 9, lines 17-18].

77. Claim 40 is rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens et al., U.S. Patent 6226729, hereinafter referred to as Stevens, in view of Johnson et al., U.S. Patent 5577236, hereinafter referred to as Johnson.

78. Stevens taught an invention to configure memory devices [FIG. 1], the invention comprising of a memory controller including a memory module interface [FIG. 5, item 500] with a serial presence detect memory [FIG. 5, items 570 and 572], wherein the memory controller:

- accesses the serial presence detect memory [column 2, lines 2-9];
- obtains information from serial presence detect memory that includes at least one characteristic of the memory module [column 12, lines 2-9]; and
- selects an operating speed for memory module interface in accordance with the obtained information [column 13, lines 41-45].

79. However, Stevens did not expressly disclose the specific characteristic to be considered or the reading of data from the memory modules.

80. Johnson taught an invention to read from a variable number of memory devices [FIG. 3], the invention comprising of generating multiple clock frequencies to provide selectable operating

speeds for the memory module interface [FIG. 4; column 7, lines 34-39; lines 53-59] based on the number of components in a memory module [column 9, lines 9-10].

81. An ordinary artisan at the same time the invention was made would have been motivated to look for a way to accurately read data from a memory that may vary in numbers and other attributes [see Johnson: column 2, line 46 to column 3, line 50].

82. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Stevens and Johnson because of the aforementioned motivation and also their involvement in similar problems regarding the configuration and operation of a system comprising of a variable number of memory devices.

83. Claims 41-42 are rejected under 35 U.S.C. 103(a) as being unpatentable over Stevens et al., U.S. Patent 6226729, hereinafter referred to as Stevens, in view of Johnson et al., U.S. Patent 5577236, hereinafter referred to as Johnson.

84. As per claim 41, Stevens taught an invention to configure memory devices [FIG. 1], the invention comprising of a memory controller including a memory module interface [FIG. 5, item 500] with a serial presence detect memory [FIG. 5, items 570 and 572], wherein the memory controller:

- accesses the serial presence detect memory [column 2, lines 2-9];
- obtains information from serial presence detect memory that includes at least one characteristic of the memory module [column 12, lines 2-9]; and
- selects an operating speed for memory module interface in accordance with the obtained information [column 13, lines 41-45].

85. However, Stevens did not expressly disclose generating multiple clock frequencies to be selected or the reading of data from the memory modules.

86. Johnson taught an invention to read from a variable number of memory devices [FIG. 3], the invention comprising of generating multiple clock frequencies to provide selectable operating speeds for the memory module interface [FIG. 4; column 7, lines 34-39; lines 53-59].

87. An ordinary artisan at the same time the invention was made would have been motivated to look for a way to accurately read data from a memory that may vary in numbers and other attributes [see Johnson: column 2, line 46 to column 3, line 50]. Generating multiple clock frequencies to be ready for selection would also alleviate any transitional delays associated with decreasing or increasing a current frequency to the desired frequency.

88. Accordingly, it would have been obvious to one of ordinary skill in the art at the time the invention was made to combine the teachings of Stevens and Johnson because of the aforementioned motivations and also their involvement in similar problems regarding the configuration and operation of a system comprising of a variable number of memory devices.

89. As per claim 42, Johnson taught the characteristic comprising of a speed grade of memory module [column 9, lines 17-18].

Conclusion

90. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

a. Chesley et al., U.S. Patent 5394541, disclosed an invention generating memory module interface signals comprising of clock, address, and data signals.

b. Aldereguia et al., U.S. Patent 5522064, disclosed an invention to dynamically configure the timing for a memory system.

c. Lee, U.S. Patent 6530001, disclosed an invention to control memory timing based on detection of memory module.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Tse Chen whose telephone number is (703) 305-8580. The examiner can normally be reached on Monday - Friday 9AM - 5PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Thomas Lee can be reached on (703) 305-9717. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Tse Chen
March 11, 2004

THOMAS LEE
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100